

ADCA / MCA (III Year)
Term-End Examination
June, 2007

CS-12 (S) : COMPUTER ARCHITECTURE

Time : 3 hours

Maximum Marks : 75

Note : Question number 1 is **compulsory**. Answer any **three** questions from the rest.

1. (a) Analyze the data dependences among the following statements in a given program :

S1 : Load R1, M(100)

S2 : Move R2, R1

S3 : Inc R1

S4 : Add R2, R1

S5 : Store M(100), R1

Are there any resource dependences if only one copy of each functional unit is available in the CPU ?

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- (b) Explain the applicability and restrictions involved in using Amdahl's law to estimate the speedup performance of an n-processor system compared with that of a single-processor system. 6
- (c) Compare the instruction set architecture in RISC and CISC processors in terms of instruction formats, addressing modes and cycles per instruction. 6
- (d) Consider the following reservation table for a four-stage pipeline with a clock cycle $\tau = 20$ ns.

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

- (i) What are the forbidden latencies and initial collision vector? 8
- (ii) Determine the MAL associated with the shortest greedy cycle. 8
- (e) Distinguish between static dataflow computers and dynamic dataflow computers. 3
2. (a) Explain two snoopy bus protocols to achieve data consistencies among the caches and shared memory. 10
- (b) What are the problems encountered in scaling up a computer to massively parallel systems? 5

3. (a) What is the purpose of prefetch buffers in instruction pipelining ? What are the other kinds of buffers used ? Give one application each of these buffers. 5

(b) A two level memory system has 8 virtual pages on a disk to be mapped into 4-page frame in main memory. The page trace is given as :

2, 0, 3, 3, 5, 5, 4, 0, 2, 5, 3, 4

Using LRU replacement policy, compute the hit ratio in the main memory. Assume the page frame initially has

3, 2, 0, 4

(c) Define the following models : 4

- (i) Shared variable model
- (ii) Message passing model

4. (a) Consider a cache (M1) and memory (M2) hierarchy with the following characteristics : 10

M1 : 16 K words, 50 ns access time

M2 : 1 M words, 400 ns access time

Assume 8-word cache blocks and a set size of 256 words with set associative mapping.

- (i) Show the mapping between M2 and M1.
- (ii) Calculate the effective memory access time with a cache hit ratio of $h = 0.95$.

(b) Explain any two differences between coarse grain and medium grain level parallelism. 5

5. (a) Make a data flow graph of the following expression evaluation : 6
$$F = (a + b) * (a - c) / (d - e)$$
- (b) What are the differences between string reduction and graph reduction machines ? 5
- (c) What are the factors limiting the degree of superscalar design ? 4