BACHELOR OF COMPUTER APPLICATIONS (BCA)

(Revised Syllabus)

BCA(Revised Syllabus)/ASSIGN/SEMESTER-II

ASSIGNMENTS

(July - 2026 & January - 2027)

ECO-02, MCS-011, MCS-012, MCS-015, MCS-013, BCSL-021, BCSL-022,

SCHOOL OF COMPUTER AND INFORMATION SCIENCES
INDIRA GANDHI NATIONAL OPEN UNIVERSITY
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Important Notes

1. Submit your assignments to the Coordinator of your Study Centre on or before the due date.
2. Assignment submission before due dates is compulsory to become eligible for appearing in corresponding Term End Examinations. For further details, please refer to BCA Programme Guide.
3. To become eligible for appearing the Term End Practical Examination for the lab courses, it is essential to fulfill the minimum attendance requirements as well as submission of assignments (on or before the due date). For further details, please refer to the BCA Programme Guide.

Course Code	**:**	**MCS-012**
Course Title	**:**	**Computer Organization and Assembly Language Programming**
Assignment Number	**:**	**BCA(II)/012/Assignment/2026-27**
Maximum Marks	**:**	**100**
Weightage	**:**	**25%**
Last Dates for Submission	**:**	**31st October, 2026 (For July 2026 Session)**
	:	**30th April, 2027 (For January 2027 Session)**

There are four questions in this assignment, which carries 80 marks. Rest 20 marks are for viva voce. You may use illustrations and diagrams to enhance the explanations. Please go through the guidelines regarding assignments given in the Programme Guide for the format of the presentation. The answer to each part of the question should be confined to about 300 words. Make suitable assumptions, if any.

Q1:

(a) Please refer to Figure 4 of Unit 1 of Block 1 on page 11 of the Instruction execution example. Assuming a similar machine is to be used for the execution of the following three consecutive instructions:

LOAD A ; Load the content of Memory location A into the Accumulator Register.
ADD B ; Add the content of memory location B to Accumulator Register.
STOR C ; Stores the content of the Accumulator register to memory location C.

However, this machine is different from the example of Figure 4 in the following ways:

- Each memory word of this new machine is of 32 bits in length.
- Each instruction is of length 32 bits with 8 bits for operation code (opcode) and 24 bits for specifying one direct operand. The size of operand is 32 bits.
- The Main Memory of the machine is of size 2^{24} words.
- The three consecutive instructions are placed starting from memory location $(C450AF)_h$; operand A is at location $(F01000)_h$ and contains a value $(11AB234F)_h$, Operand B is at location $(F01001)_h$ and contains a value $(11122350)_h$ and operand C is at location $(F01001)_h$ and contains a value $(00000000)_h$.
- The AC, IR, MAR and MBR registers are of size 32 bits, whereas PC register is of size 24 bits. The initial content of the PC register is $(C450AF)_h$.

(i) Draw a diagram showing the Initial State of the machine with the addresses and content of memory locations in hexadecimal. Show only those address locations of the memory that store the instruction and data. Also, show the content of all the stated registers. **(2 Marks)**

(ii) Draw three more diagrams, each showing the state of the machine after execution of every instruction viz. LOAD, ADD and STOR. Show the changes in the values of Registers and memory locations, if any, due to the execution of the instruction. Show all the addresses and values in hexadecimal notations. **(3 Marks)**

(b) Perform the following conversion of numbers: **(2 Marks)**

i) Decimal $(3456345123)_{10}$ to binary and hexadecimal
ii) Hexadecimal $(CABFF114)_h$ into Octal.

iii) String "Convert This String $%" into UTF-8.
iv) Octal $(5674312)_O$ into Decimal

(c) Simplify the following function using K-map: $F(A, B, C, D) = \Sigma (0, 1, 3, 5, 8, 10, 13, 14)$
Also, draw the circuit for the simplified function using NAND gates. **(2 Marks)**

(d) Consider the Adder-Subtractor circuit as shown in Figure 3.15, page 76 of Block 1. What would be the values of various inputs and outputs, viz. C_{in} input to each full adder, A_0, B_0, A_1, B_1, A_2, B_2, A_3, B_3, S_0, S_1, S_2, S_3, Carry out bit, and overflow condition; if this circuit performs a subtraction operation (A-B), when the value of A is 0001, and B is 1001. **(1 Marks)**

(e) Explain the functioning of a 2 × 4 decoder with the help of a logic diagram and an example input. **(2 Marks)**

(f) Assume that a source data value 0001 was received at a destination as 0011. Show how Hamming's Error-Correcting code bits will be appended to the source data to identify and correct the error of one bit at the destination. You may assume that a transmission error has occurred in the source data and not the source parity bits. **(2 Marks)**

(g) Explain the functioning of the RS flip flop with the help of a logic diagram and characteristic table. Also, explain the excitation table of this flip-flop. **(2 Marks)**

(h) Explain the edge-triggered flip-flop with the help of suitable diagrams. **(2 Marks)**

(i) Represent $(155.125)_{10}$ and $(-9.25)_{10}$ in IEEE 754 single-precision and double-precision formats. **(2 Marks)**

Q2:

(a) Refer to the Figure 2(b) on page 8 in Unit 1 of Block 2. Draw the Internal organisation of a 4×4 RAM. Explain all the inputs and outputs of this organisation. Also, answer the following: **(2 Marks)**

(i) How many data input and data output lines does this RAM needs? Explain your answer.
(ii) How many address lines are needed for this RAM? Give reason in support of your answer.

(b) A computer has 4 K Word RAM with each memory word of 8 bits. It has a cache memory having 8 blocks of size 32 bits each (4 memory words). Show how the main memory address $(2AC)_h$ will be mapped to the cache address, if **(3 Marks)**

(i) Direct cache mapping is used
(ii) Associative cache mapping is used
(iii) Two way set associative cache mapping is used.

You should show the size of tag, index, main memory block address and offset in your answer.

(c) What is an Interrupt in a computer system? What is the importance of an interrupt? Give two examples of interrupts that can occur in a computer system. When is an interrupt acknowledged in a computer? Explain. **(3 Marks)**

(d) What is DMA? How is it different from Programmed I/O? Explain the working of a DMA with the help of a diagram. **(2 Marks)**

(e) Assume that a disk has 32 tracks, with each track having 16 sectors, and each sector is of size 1 M Bytes. The cluster size in this system can be assumed to be 2 sectors. A file named *bca.txt* of size 8 MB in size, is to be stored on this disk. Assume it is a new disk, with the first 4 clusters occupied by the Operating System and the remaining clusters are free. How can this file be allotted space on this disk? Also, show the FAT contents after the space allocation to this file. You may make suitable assumptions. **(4 Marks)**

(f) Explain the following giving their uses and advantages/disadvantages, if needed.
(Word limit for answer of each part is 50 words ONLY) **(6 Marks)**

(i) Access time on a Hard disk
(ii) Impact Printers
(iii) MODEM
(iv) LCD monitors

Q3:

(a) A single-core uniprocessor system has 8 general-purpose registers. The machine has 4 KB of RAM, consisting of 32-bit memory words. The size of every general-purpose register and memory word is 32 bits. The computer uses 32-bit fixed-length instructions. A machine instruction of this machine can have two operands. One of these operands is a direct memory operand, and the other is a register operand. An instruction of a machine consists of bits for the operation code, bits for the memory operand and bits for the register operand. The machine has 64 different operation codes. The machine also has special-purpose registers, which are other than general-purpose registers. These special-purpose registers are: Program Counter (PC), Memory Address Register (MAR), Data Register (DR), and Flag registers (FR). The first general-purpose register can be used as the Accumulator Register. The size of Integer operands on the machine may be assumed to be equal to the size of the accumulator register. To execute instructions, the machine has another special-purpose register, the 32-bit Instruction Register (IR), since each instruction is of 32 bits. Perform the following tasks for the machine. (Make and state suitable assumptions, if any.)

(i) Design suitable instruction formats for the machine. Specify the sizes of the different fields needed in an instruction format. Also, indicate how many bits of an instruction are unused for this machine. Explain your design of the instruction formats. What would be the size of each register? **(3 Marks)**

(ii) Illustrate two valid instructions of the machine by drawing a diagram that shows instructions and related data in registers and memory. **(2 Marks)**

(iii) Assuming that an instruction is first fetched to the Instruction Register (IR), its memory operand is brought to the DR register, and the result of an operation is stored in the Accumulator register, write and explain the sequence of micro-operations to fetch and execute an addition instruction that adds the contents of a direct memory operand to the contents of a register operand. The result is stored in the accumulator register. Make and state suitable assumptions, if any. **(5 Marks)**

(b) Assume that you have a machine, as shown in section 3.2.2 of Block 3, having the set of micro-operations as given in Figure 10 on page 62 of Block 3. Consider that R1 and R2 are both 8-bit registers and contain 00011001 and 11101100, respectively. What will be the values of select inputs, carry-in input, and the result of the operation (including carry-out bit) if the following

micro-operations are performed on these registers? (For each micro-operation, you may assume the initial value of R1 and R2 as given above.) **(2 Marks)**

(i) Decrement R1
(ii) Add R1 and R2
(iii) AND R1 with R2
(iv) Shift left R1

(c) Consider that an instruction pipeline has four stages, namely Instruction Fetch (INF), Instruction Decode (IND), Operand Fetch (OPF), and Execute & Store Results (ESR). Draw an instruction pipeline diagram showing the execution of six sequential instructions using this pipeline. Explain what problem may occur if the 2nd instruction is a conditional jump instruction? **(3 Marks)**

(d) Explain the Horizontal and Vertical micro-instructions with the help of a diagram of each. **(2 Marks)**

(e) What is RISC Architecture? What are the advantages of a RISC machine over a CISC machine? What are its drawbacks? Explain the RISC pipelining with the help of a diagram. **(3 Marks)**

Q4:

(a) Write a program using 8086 assembly Language (with appropriate comments) that reads a binary value stored in a byte memory location and displays its corresponding ASCII digit on the screen, provided that the binary value is less than $(00001010)_2$. Make suitable assumptions, if any. For example, if the byte memory location contains $(00000011)_2$, then the program should display the ASCII digit '3'. **(7 Marks)**

(b) What is a NEAR procedure call in the 8086 microprocessor? How is it different from a FAR procedure call in an 8086 microprocessor? Assuming that a stack is used for implementing procedure calls, explain how two parameters of byte type are passed to a NEAR procedure using the stack and how they can be accessed within the procedure. You do not need to write assembly code; instead, draw the necessary diagrams to illustrate the concept. **(7 Marks)**

(c) Explain the following in the context of 8086 Microprocessor with the help of an example or a diagram: **(6 Marks)**

(i) Use of Segment Registers in Address computation.
(ii) Use of the carry flag, sign flag, overflow flag and zero flag
(iii) Instructions – MUL, TEST, SHL, ROR