Course Code	**:**	**MCS-012**
Course Title	**:**	**Computer Organisation and Assembly Language Programming**
Assignment Number	**:**	**BCA(II)/012/Assignment/2024-25**
Maximum Marks	**:**	**100**
Weightage	**:**	**25%**
Last Dates for Submission	**:**	**31st October, 2024 (For July Session)** **30th April, 2025 (For January Session)**

There are four questions in this assignment, which carries 80 marks. Rest 20 marks are for viva voce. You may use illustrations and diagrams to enhance the explanations. Please go through the guidelines regarding assignments given in the Programme Guide for the format of the presentation. The answer to each part of the question should be confined to about 300 words. Make suitable assumptions, if any.

Question 1:

(a) Please refer to Figure 4 of Unit 1 of Block 1 on page 11 of the Instruction execution example. Assuming a similar machine is to be used for the execution of the following three consecutive instructions:
LOAD A ; Load the content of Memory location A into the Accumulator Register.
ADD B ; Add the content of memory location B to Accumulator Register.
STOR C ; Stores the content of the Accumulator register to memory location C.
However, this machine is different from the example in Figure 4 in the following ways:

- Each memory word of this new machine is of 32 bits length.
- Each instruction is of length 32 bits with 12 bits for operation code (opcode) and 20 bits for specifying one direct operand. The size of operand is 32 bits.
- The Main Memory of the machine is of size 2^{20} words.
- The three consecutive instructions are placed starting from memory location $(11FFE)_h$; operand A is at location $(2FFFF)_h$ and contains a value $(111AB4C1)_h$, Operand B is at location $(30000)_h$ and contains a value $(AAA1A1FE)_h$ and operand C is at location $(30001)_h$ and contains a value $(00000000)_h$.
- The AC, IR, MAR and MBR registers are of size 32 bits, whereas PC register is of size 20 bits. The initial content of the PC register is $(11FFE)_h$.

(i) Draw a diagram showing the Initial State of the machine with the addresses and content of memory locations in hexadecimal. Show only those address locations of the memory that store the instruction and data. Also, show the content of all the stated registers. **(2 Marks)**

(ii) Draw three more diagrams, each showing the state of the machine after execution of every instruction viz. LOAD, ADD and STOR. Show the changes in the values of Registers and memory locations, if any, due to the execution of the instruction. Show all the addresses and values in hexadecimal notations. **(3 Marks)**

(b) Perform the following conversion of numbers: **(2 Marks)**

i) Decimal $(345789531)_{10}$ to binary and hexadecimal.
ii) Hexadecimal $(ABC023DEF)_h$ into Octal.
iii) String "MCS-12 Price in $" into UTF 8.
iv) Octal $(12076543)_O$ into Decimal.

(c) Simplify the following function using K-map: $F(A, B, C, D) = \Sigma (0, 1, 2, 4, 8, 9, 10, 13)$
Draw the circuit for the resultant function using NAND gates. **(2 Marks)**

(d) Consider the Adder-Subtractor circuit as shown in Figure 3.15 page 76 of Block 1. What would be the values of various inputs and outputs; viz. C_{in} input to each full adder, A_0, B_0, A_1, B_1, A_2, B_2, A_3, B_3, S_0, S_1, S_2, S_3, Carry out bit, and overflow condition; if this circuit performs subtraction (A-B), when the value of A is 1010 and B is 1011. **(1 Mark)**

(e) Explain the functioning of a 2 × 4 decoder with the help of a logic diagram and an example input. **(2 Marks)**

(f) Assume that a source data value 1111 was received at a destination as 1011. Show how Hamming's Error-Correcting code bits will be appended to source data to identify and correct the error of one bit at the destination. You may assume that transmission error occurs only in the source data and not the source parity bits. **(2 Marks)**

(g) Explain the functioning of the RS flip flop with the help of a logic diagram and characteristic table. Also, explain the excitation table of this flip-flop. **(2 Marks)**

(h) Explain the functioning of the master-slave flip-flop with the help of a diagram. **(2 Marks)**

(i) Represent $(129.5)_{10}$ and $(-1.125)_{10}$ in IEEE 754 single-precision and double-precision formats. **(2 Marks)**

Question 2:

(a) Refer to the Figure 2(b) on page 8 in Unit 1 of Block 2. Draw the Internal organisation of a 16×2 RAM. Explain all the Input and Output of this organisation. Also, answer the following:

(i) How many data input and data output lines does this RAM need? Explain your answer.
(ii) How many address lines are needed for this RAM? Give reasons in support of your answer.
(2 Marks)

(b) A computer has 4 K Word RAM with each memory word of 8 bits. It has cache memory, having 16 blocks, having a size of 16 bits (2 memory words). Show how the main memory address $(3AC)_h$ will be mapped to the cache address, if
(i) Direct cache mapping is used
(ii) Associative cache mapping is used
(iii) Two-way set associative cache mapping is used.
You should show the size of the tag, index, main memory block address and offset in your answer. **(3 Marks)**

(c) What are the different kinds of interrupts? Explain the process of handling an interrupt with the help of a diagram. . **(3 Marks)**

(d) What is a DMA? What are the advantages of using DMA? Explain the functions of a DMA interface with the help of a block diagram. **(2 Marks)**

(e) Assume that a disk has 128 tracks, with each track having 64 sectors and each sector is of size 1 M Bytes. The cluster size in this system can be assumed to be 2 sectors. A file having the name *assignmentmcs012.txt* is of size 16 MB. Assume that it is a new disk, and the first 16 clusters are occupied by the Operating System. Rest all the clusters are free. How can this file be allotted space on this disk? Also, show the content of FAT after the space allocation to this file. You may make suitable assumptions. **(4 Marks)**

(f) Explain the following, giving their uses and advantages/disadvantages, if needed. (Word limit for the answer of each part is 50 words ONLY**)** **(6 Marks)**

- **(i)** Access time of disks
- **(ii)** CD-ROM
- **(iii)** Classification of Printers
- **(iv)** Scanner
- **(v)** Refresh rates of monitors
- **(vi)** Devices for data backup

Question 3:

(a) A single-core uniprocessor system has 16 General purpose registers. The machine has RAM of size 1 M memory words. The size of every general-purpose register and memory word is 32 bits. The computer uses fixed-length instructions of size 32 bits each. An instruction of the machine can have two operands. One of these operands is a direct memory operand and the other is a register operand. An instruction of a machine consists of bits for operation code, bits for memory operand and bits of register operand. The machine has about 64 different operation codes. The machine also has special purpose registers, which are other than general purpose registers. These special purpose registers are – Program Counter (PC), Memory Address Register (MAR), Data Register (DR) and Flag registers (FR). The first register among the general-purpose registers can be used as Accumulator Register. The size of Integer operands on the machine may be assumed to be equal to the size of the accumulator register. To execute instructions, the machine has another special purpose register called Instruction Register (IR) of size 32 bits, as each instruction is of this size. Perform the following tasks for the machine. (Make and state suitable assumptions, if any.)

(i) Design suitable instruction formats for the machine. Specify the size of different fields that are needed in the instruction format. Also, indicate how many bits of the instructions are unused for this machine. Explain your design of the instruction format. What would be the size of each register?

(3 Marks)

(ii) Illustrate two valid instructions of the machine by drawing a diagram that shows instructions and related data in registers and memory. **(2 Marks)**

(iii) Assuming that an instruction is first fetched to the Instruction Register (IR), its memory operand is brought to the DR register and the result of an operation is stored in the Accumulator register, write and explain the sequence of micro-operations to fetch and execute an addition instruction that adds the contents of a memory operand with the contents of a register operand. The result is stored in the accumulator register. Make and state suitable assumptions, if any. **(5 Marks)**

(b) Assume that you have a machine, as shown in section 3.2.2 of Block 3 having the set of micro-operations as given in Figure 10 on page 62 of Block 3. Consider that R1 and R2 both are 8-bit registers and contain 01111110 and 11010101 respectively. What will be the values of select inputs, carry-in input, and the result of the operation (including carry-out bit) if the following micro-operations are performed on these registers? (For each micro-operation you may assume the initial value of R1 and R2 as given above)

(2 Marks)

- **(i)** Increment R2
- **(ii)** Subtract R2 from R1
- **(iii)** AND of R1 with R2
- **(iv)** Shift left R1

(c) Consider that an instruction pipeline has four stages namely instruction fetch (INFE), Instruction decode and Operand Fetch (IDOF), Instruction Execute (INEX) and store results (STRE). Draw an instruction pipeline diagram showing the execution of five sequential instructions using this pipeline. Explain, what problem may occur, if the 2nd instruction is a conditional jump instruction? **(3 Marks)**

(d) Explain the structure and operation of the micro-programmed control unit with the help of a diagram. **(2 Marks)**

(e) Explain the use of large register file in RISC. Also, explain the optimisation of RISC pipelining. **(3 Marks)**

Question 4:

(a) Write a program using 8086 assembly Language (with proper comments) that accepts two different digits as input from the keyboard. Each digit is converted to its binary equivalent value. These converted digits are stored in registers BL and CL. The program then stores the smaller of these two values in AL register. The program also checks if the present AL value is larger than all the values contained in a byte array of size 6, which is stored in the memory. If so, then a value 1 is moved to DL register, else a value 0 is moved to DL register. You may assume the byte array has the values 02h, 03h, 05h, 01h, 02h, 03h. Make suitable assumptions, if any. **(7 Marks)**

(b) Differentiate between the FAR and NEAR procedure calls in 8086 micro-processor. Assuming that a stack is used for implementing procedure calls, explain how call and return statements of 8086 microprocessor would use stack for NEAR and FAR procedure calls and return from a call. Also, assuming that two parameters are to be passed to a procedure using stack, explain how they will be passed to the procedure and accessed in the procedure. You need not write the assembly code but draw necessary diagrams to illustrate the concept. **(7 Marks)**

(c) Explain the following in the context of 8086 Microprocessor with the help of an example or a diagram: **(6 Marks)**

- **(i)** Explain the use of Segment Registers in 8086 microprocessor
- **(ii)** Explain the use of the flags - CF, ZF, OF, DF
- **(iii)** Explain the Instructions – XLAT, MUL, SAR, RCL