BACHELOR OF COMPUTER APPLICATIONS (BCA)

(Revised Syllabus)

ASSIGNMENTS

(July - 2025 & January – 2026 sessions)

ECO-02, MCS-011, MCS-012, MCS-015, MCS-013, BCSL-021, BCSL-022

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THE PEOPLE'S UNIVERSITY

SCHOOL OF COMPUTER AND INFORMATION SCIENCES
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Important Notes

1. Submit your assignments to the Coordinator of your Study Centre on or before the due date.

2. Assignment submission before due dates is compulsory to become eligible for appearing in corresponding Term End Examinations. For further details, please refer to BCA Programme Guide.

3. To become eligible for appearing the Term End Practical Examination for the lab courses, it is essential to fulfill the minimum attendance requirements as well as submission of assignments (on or before the due date). For further details, please refer to the BCA Programme Guide.

There are four questions in this assignment, which carry 80 marks. Rest 20 marks are for viva voce. You may use illustrations and diagrams to enhance the explanations. Please go through the guidelines regarding assignments given in the Programme Guide for the format of the presentation. The answer to each part of the question should be confined to about 300 words. Make suitable assumptions, if any.

Question 1:
(a) Please refer to Figure 4 of Unit 1 of Block 1 on page 11 of the Instruction execution example. Assuming a similar machine is to be used for the execution of the following three consecutive instructions:

  LOAD A; Load the content of Memory location A into the Accumulator Register.
  SUBT B; Subtract the content of memory location B from the Accumulator Register.
  STOR C; Stores the content of the Accumulator register to memory location C.

  However, this machine is different from the example in Figure 4 in the following ways:
  • Each memory word of this new machine is 16 bits long.
  • Each instruction is of length 16 bits with 4 bits for the operation code (opcode) and 12 bits for specifying one direct operand. The size of an operand is 16 bits.
  • The Main Memory of the machine is of size 2^{12} words.
  • The three consecutive instructions are placed starting from memory location $(10F)_h$; operand A is at location $(2FF)_h$ and contains a value $(2AC5)_h$, Operand B is at location $(300)_h$ and contains a value $(1AEE)_h$ and operand C is at location $(301)_h$ and contains a value $(00000)_h$.
  • The AC, IR, MAR and MBR registers are of size 16 bits, whereas the PC register is of size 12 bits. The initial content of the PC register is $(10E)_h$.

  (i) Draw a diagram showing the Initial State of the machine with the addresses and content of memory locations in hexadecimal. Show only those address locations of the memory that store instructions and data. Also, show the content of all the stated registers.
                                                                                                          (2 Marks)
  (ii) Draw three more diagrams, each showing the state of the machine after execution of every instruction, viz. LOAD, SUBT and STOR. Show the changes in the values of Registers and memory locations, if any, due to the execution of the instruction. Show all the addresses and values in hexadecimal notation.
                                                                                                          (3 Marks)

(b) Perform the following conversion of numbers: **(2 Marks)**
  i)   Decimal $(269785421)_{10}$ to binary and hexadecimal.
  ii) Hexadecimal $(8FACBED34)_h$ into Octal.
  iii) String "lowercase vs UPPERCASE" into UTF-8.
  iv) Octal $(65874531)_O$ into Decimal.

(c) Simplify the following function using K-map: F (A, B, C, D) = Σ (0, 2, 6, 8, 9, 12). Also, draw the circuit for the simplified function using NAND gates. **(2 Marks)**

(d) Consider the Adder-Subtractor circuit as shown in Figure 3.15, page 76 of Block 1. What would be the values of various inputs and outputs, viz. C_{in} input to each full adder, A_0, B_0, A_1, B_1, A_2, B_2, A_3, B_3, S_0, S_1, S_2, S_3, Carry out bit, and overflow condition; if this circuit performs subtraction operation (A-B), when the value of A is 0011 and B is 1111. **(1 Mark)**

(e) Explain the functioning of a 4×1 multiplexer with the help of a logic diagram and an example input. **(2 Marks)**

(f) Assume that a source data value 1001 was received at a destination as 1000. Show how Hamming's Error-Correcting code bits will be appended to source data to identify and correct the error of one bit at the destination. You may assume that a transmission error has occurred in the source data and not the source parity bits. **(2 Marks)**

(g) Explain the functioning of the JK flip-flop with the help of a logic diagram and characteristic table. Also, explain the excitation table of this flip-flop. **(2 Marks)**

(h) Draw the block diagram of a master-slave flip-flop and explain its functioning. **(2 Marks)**

(i) Represent $(321.25)_{10}$ and $(-7.125)_{10}$ in IEEE 754 single-precision and double-precision formats. **(2 Marks)**

Question 2:

(a) Refer to the Figure 2(b) on page 8 in Unit 1 of Block 2. Draw the Internal organisation of an 8×4 RAM. Explain all the inputs and outputs of this organisation. Also, answer the following:
(i) How many data input and data output lines does this RAM need? Explain your answer.
(ii)How many address lines are needed for this RAM? Give reasons in support of your answer. **(2 Marks)**

(b) A computer has 4 K Word RAM with each memory word of 16 bits. It has cache memory having 8 blocks of size 32 bits (2 memory words). Show how the main memory address $(1A9)_h$ will be mapped to the cache address, if
(i) Direct cache mapping is used
(ii) Associative cache mapping is used
(iii)Two-way set-associative cache mapping is used.
You should show the size of the tag, index, main memory block address and offset in your answer. **(3 Marks)**

(c) Define the term Interrupt? Why is an interrupt used in a computer? How is an interrupt handled? Explain with the help of a suitable diagram. **(3 Marks)**

(d) What is an Input/Output processor? What are the uses of the Input/Output processor? Explain the structure of the Input/Output processor/channel with the help of a diagram. **(2 Marks)**

(e) Assume that a disk has 64 tracks, with each track having 32 sectors, and each sector is of size 4 M Bytes. The cluster size in this system can be assumed to be 4 sectors. A file having the name *assignmentbca.txt*, of

size 32 MB, is to be stored on this disk. Assume that it is a new disk, and the first 4 clusters are occupied by the Operating System, and the rest of the clusters are free. How can this file be allotted space on this disk? Also, show the content of FAT after the space allocation to this file. You may make suitable assumptions. **(4 Marks)**

(f) Explain the following, giving their uses and advantages/disadvantages, if needed.
   (Word limit for the answer of each part is 50 words ONLY) **(6 Marks)**
   (i) Latency time of the Hard disk
   (ii) Non-impact Printers
   (iii) MODEM
   (iv) Video Memory
   (v) Colour depth of monitors
   (vi) Magnetic Tape

Question 3:

(a) A single-core uniprocessor system has 32 general-purpose registers. The machine has a RAM of size 64 KB memory words. The size of every general-purpose register and memory word is 32 bits. The computer uses fixed-length instructions of size 32 bits each. An instruction of the machine can have two operands. One of these operands is a direct memory operand, and the other is a register operand. An instruction of a machine consists of bits for the operation code, bits for the memory operand and bits for the register operand. The machine has 32 different operation codes. The machine also has special-purpose registers, which are other than general-purpose registers. These special-purpose registers are – Program Counter (PC), Memory Address Register (MAR), Data Register (DR) and Flag registers (FR). The first register among the general-purpose registers can be used as the Accumulator Register. The size of Integer operands on the machine may be assumed to be equal to the size of the accumulator register. To execute instructions, the machine has another special-purpose register called the Instruction Register (IR) of size 32 bits, as each instruction is of this size. Perform the following tasks for the machine. (Make and state suitable assumptions, if any.)

   (i) Design suitable instruction formats for the machine. Specify the size of different fields that are needed in an instruction format. Also, indicate how many bits of an instruction are unused for this machine. Explain your design of the instruction formats. What would be the size of each register?
   (3 Marks)
   (ii) Illustrate two valid instructions of the machine by drawing a diagram that shows instructions and related data in registers and memory. **(2 Marks)**

   (iii) Assuming that an instruction is first fetched to the Instruction Register (IR), its memory operand is brought to the DR register and the result of an operation is stored in the Accumulator register, write and explain the sequence of micro-operations to fetch and execute a subtraction instruction that subtracts the contents of a memory operand from the contents of a register operand. The result is stored in the accumulator register. Make and state suitable assumptions, if any.
   (5 Marks)

(b) Assume that you have a machine, as shown in section 3.2.2 of Block 3, having the set of micro-operations as given in Figure 10 on page 62 of Block 3. Consider that R1 and R2 are both 8-bit registers and contain 10010001 and 00100100, respectively. What will be the values of select inputs, carry-in input, and the result of the operation (including carry-out bit) if the following micro-operations are performed on these registers? (For each micro-operation, you may assume the initial value of R1 and R2 as given above)
   (2 Marks)

   (i) Decrement R2
   (ii) Add R1 and R2
   (iii) OR R1 and R2
   (iv) Shift right R1

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(c) Consider that an instruction pipeline has three stages, namely instruction fetch and decode (FED), Operand Fetch and Execute (OFX) and store results (STOR). Draw an instruction pipeline diagram showing the execution of five sequential instructions using this pipeline. Explain what problem may occur if the 1st instruction is a conditional jump instruction?

(3 Marks)

(d) Explain the structure and operation of the Wilkes control Unit. Compare the Wilkes control unit and micro-programmed control unit. **(2 Marks)**

(e) What are the characteristics of Reduced Instruction Set Computers (RISC)? What are the uses of a large number of Registers in RISC machines? Explain. **(3 Marks)**

Question 4:

(a) Write a program using 8086 assembly Language (with proper comments) that accepts one digit as input from the keyboard. This digit is converted to its binary equivalent value and stored in the BL register. The program stores the value of BL in the first element of a byte memory array of size 10. It then increments the BL value and stores it in the second location. This process continues, with the BL value being incremented and stored in each subsequent location of the memory array. Make suitable assumptions, if any.

(7 Marks)

(b) What is a FAR procedure call in the 8086 microprocessor? How is it different from a NEAR procedure call in an 8086 microprocessor? Assuming that a stack is used for implementing procedure calls, and three-word parameters are passed to a FAR procedure, explain how they will be passed and accessed in the procedure. You need not write the assembly code but draw the necessary diagrams to illustrate the concept.

(7 Marks)

(c) Explain the following in the context of the 8086 Microprocessor with the help of an example or a diagram:
(6 Marks)
   (i) Explain the use of CS and IP registers for computing the address of an instruction in the memory and SS and SP registers for computing the address of the top of the stack.
   (ii) Explain the use of the following flags - CF, SF, PF, IF
   (iii) Explain the Instructions – LEA, CMP, SHR, RCR