POST GRADUATE DIPLOMA IN COMPUTER APPLICATIONS

(PGDCA_NEW)

PGDCA_NEW/ASSIGN/SEMESTER-I

ASSIGNMENTS

(January – 2026 & July – 2026)

MCS-201, MCS-202, MCS-203, MCSL-204, MCSL-205

SCHOOL OF COMPUTER AND INFORMATION SCIENCES
INDIRA GANDHI NATIONAL OPEN UNIVERSITY
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Important Notes

1. Submit your assignments to the Coordinator of your Study Centre on or before the due date.
2. Assignment submission before due dates is compulsory to become eligible for appearing in corresponding Term End Examinations. For further details, please refer to PGDCA_NEW Programme Guide.
3. To become eligible for appearing the Term End Practical Examination for the lab courses, it is essential to fulfill the minimum attendance requirements as well as submission of assignments (on or before the due date). For further details, please refer to the PGDCA_NEW Programme Guide.
4. The viva voce is compulsory for the assignments. For any course, if a student submitted the assignment and not attended the viva-voce, then the assignment is treated as not successfully completed and would be marked as ZERO.

Course Code	**:**	**MCS-202**
Course Title	**:**	**Computer Organisation**
Assignment Number	**:**	**PGDCA_NEW(I)/202/Assignment/2026**
Maximum Marks	**:**	**100**
Weightage	**:**	**30%**
Last Dates for Submission	**:**	**30th April, 2026 (for January session)**
		31st October, 2026 (for July session)

There are four questions in this assignment, which carries 80 marks. The remaining 20 marks are for viva voce. You may use illustrations and diagrams to enhance the explanations. Please go through the guidelines regarding assignments given in the Programme Guide for the presentation format. The answer to each part of the question should be confined to about 300 words. Make suitable assumptions, if any.

Question 1: (covers Block1) **(2 marks each × 10 parts =20 Marks)**

(a) Explain the von Neumann architecture with the help of a diagram. Also, explain how the data and instructions are stored in this architecture.

(b) Explain how a computer will execute the following high-level language program segment:

```
int x=10, y=20, result;
result=x+y;
```

(c) Perform the following conversion of numbers:

(i) Decimal $(1479865320)_{10}$ to binary and hexadecimal.

(ii) Hexadecimal $(BCDAFD01)_h$ to binary and Octal.

(iii) ASCII String "BCA Programme Code is BCA_NEW & BCA_NEWOL" to UTF-8

(iv) Octal $(72143065)_O$ to Decimal

(d) Simplify the following function using a K-map: $F(A, B, C, D) = \Sigma (1,3, 4, 5, 7, 11, 12)$. Draw the circuit for the simplified function using NAND gates.

(e) Consider the Adder-Subtractor circuit given in Unit 3 of Block 1. Explain how this circuit will perform subtraction (A-B) if the value of A is 1001 and B is 0111. You must list all the bit values, including C_{in}, C_{out}, and the overflow condition.

(f) Make the Truth Table and draw the logic diagram of a 3×8 decoder. Explain its functioning with the help of a truth table and an example input.

(g) Assume that a source data value 1011 was received at a destination as 0011. Show how Hamming's Error-Correcting code will be appended to the source data, so this one-bit error is identified and corrected at the destination. You may assume that the transmission error occurs in the source data and not in the error correction code.

(h) Explain the functioning of the RS flip-flop with the help of a logic diagram and a characteristic table. Also, make and explain the excitation table of this flip-flop.

(i) Explain the functioning of a synchronous counter.

(j) Represent $(-729.25)_{10}$ and $(0.0078125)_{10}$ in IEEE 754 single precision format.

Question 2: (covers Block 2) **(4 marks each × 5 parts =20 Marks)**

(a) (i) Explain the structure of a 4× 2 ROM with the help of a diagram. (ii) How many memory chips of size 128K × 8bits are needed to build a RAM of size 64 M words if the word size of RAM is 32 bits? (iii) Find the storage capacity of a Magnetic disk with 16 recording surfaces, and 256 tracks consisting of 256 sectors each. You may assume that each sector can store 1 MB of data. (iv) Find the rotational latency of a disk that rotates at 9000 rpm.

(b) Consider that the main memory of a computer is 256 words (assume a memory word to be 32 bits). The cache memory of this computer consists of 8 blocks, each 128 bits in size. Find the cache addresses for the main memory addresses 01100011_2 and 11010111_2 for the following cache mapping schemes:
   (i) Associative cache mapping
   (ii) Direct cache mapping
   (iii) Two-way set associative cache mapping

(c) Explain the steps of a Direct Memory Access (DMA) transfer. What are the advantages of using the DMA technique of data transfer? Illustrate the DMA breakpoints in an instruction cycle with the help of a diagram.

(d) What is an interrupt? Explain the steps of interrupt processing with the help of a diagram. Explain the design issues for implementing interrupt-driven Input/Output (I/O).

(e) Explain the features of the following I/O Technologies:
   (i) Active-Matrix Liquid Crystal Displays
   (ii) Colour Depth in the context of Video cards
   (iii) Scanners
   (iv) Non-impact printers

Question 3: (Covers Block 3) **(4 marks each × 5 parts =20 Marks)**

(a) Explain the functioning of subroutine call and return instructions with the help of an example. Also, explain indirect addressing, indexed addressing, and stack addressing with the help of an example for each.

(b) Demonstrate how the size of a machine program changes for the computation of the expression **result=(a+b) * (a*b+c)** when the instruction sets have (i) zero address instructions, (ii) one address instructions, (iii) two address instructions, and (iv) three address instructions.

(c) Consider a machine that uses PC, IR, AC, and MAR registers to execute different instructions. All the memory accesses during instruction execution bring data to a temporary register named TR. The ALU of the machine performs the subtraction operation using the AC and TR registers, and the result of the subtraction operation is stored in the AC register. List and explain all the microoperations required to execute the following machine instruction:

   AC ← AC -M; where M is the address of a direct operand in the Memory

   Assume that PC is currently pointing to this instruction.
   Make and state suitable assumptions, if any.

(d) Explain the operation of a micro-programmed control unit with the help of a diagram.

(e) What are the features of a RISC machine? Explain the RISC pipelining with the help of a diagram.

Question 4: (Covers Block 4) **(5 marks each × 4 parts =20 Marks)**

(a) What is a Flag register in the 8086 microprocessor? Explain any four flags and their use. What is the need for a segment register in the 8086 microprocessor? Compute the physical address for the following {Segment Register : Offset} pairs in an 8086 microprocessor:

(i) CS: IP = $ABCD_h$:$AAFF_h$
(ii) DS:BX = $1FBH_h$:$99FF_h$
(iii) SS: SP = $EFFF_h$: $00AB_h$

(b) What is an Interrupt Vector Table (IVT) in the 8086 microprocessor? Explain its use with the help of a diagram. Write a program using 8086 assembly language to input a string: "Welcome to the Programme."

(c) Write a program in 8086 assembly language that converts a 4-bit unsigned binary number to an equivalent unpacked BCD value. For example, the input binary number 1101_2 is first converted to its equivalent BCD value, 13, i.e., 00010011_2. This value is then unpacked and stored as unpacked BCD values, 00000001_2 and 00000011_2. Explain the algorithm of the program.

(d) Explain the features and advantages of the following:
(i) Pipeline for adding two floating-point numbers
(ii) Vector Processing
(iii) Bus interconnection structure in a multiprocessor system
(iv) Multi-core processors
(v) Inter-processor communication and synchronisation