No. of Printed Pages : 6 **MCS–012**

MASTER OF COMPUTER APPLICATIONS/BACHELOR OF COMPUTER APPLICATIONS (MCA/BCA) (REVISED)

Term-End Examination

June, 2025

MCS-012 : COMPUTER ORGANISATION AND ASSEMBLY LANGUAGE PROGRAMMING

Time : 3 Hours *Maximum Marks : 100*

Note : *(i) Question No. **1** is compulsory and carries 40 marks.*

*(ii) Attempt any **three** questions from the rest.*

1. (a) Represent the number 1110.0011 in IEEE754 floating point single precision number representation. 6

(b) Perform the following computation using binary's 2's complement notation, assuming the register size to be 8 bits. Also check for occurrence of overflow : 6

(i) – 63 + 74

(ii) – 128 + 39

(iii) + 86 + 42

(c) What is the need of cache memory ? Explain the direct cache mapping scheme with the help of an example or diagram. 6

(d) Simplify the following using Karnaugh's map : 5

$$F(A, B, C, D) = \Sigma (0, 1, 3, 5, 8, 10, 13)$$

(e) A machine uses evaluation stack architecture. Write a program for evaluation of the following expression :6

$$A = B * (C + D) * E$$

(f) Draw the block diagram of hardwired control unit and explain how does it work. 6

(g) How many chips of 512 K × 8 are required for constructing 4M × 32 memory ? 5

2. (a) Explain the following 8086 instructions : 6

(i) AND

(ii) SHL

(iii) INC

(b) Explain the use of stack for parameter passing in a subroutine/function call. 5

(c) Explain the concept of Direct Memory Access with the help of a diagram. 5

(d) Calculate the physical address for the following register offset pairs in 8086 microprocessor : 4

(i) SS : SP = 0100h : 0020h

(ii) DS : BX = 0200h : 0100h

(iii) CS : IP = 4200h : 0123h

(iv) ES : SI = 0300h : 0245h

3. (a) Explain the following terms : 6

(i) Seek time

(ii) Latency time

(iii) Hit ratio in cache

(b) Discuss the use of any *four* flags for the 8086 microprocessor. 4

(c) Explain the concept of instruction pipelining with the help of a diagram. 5

(d) Differentiate between programmed I/O and interrupt driven I/O schemes. 5

4. (a) Explain the features of RISC architecture. 6

   (b) What is an accumulator based instruction set architecture ? Write the assembly code for evaluating the expression A = B*C + D for accumulator based machine. 6

   (c) A memory chip has a capacity of 1M × 16 bits :

      (i) How many address lines does it have ? 2

      (ii) What is the capacity of the chip in bytes ? 2

   (d) Discuss the use of a device driver. 4

5. (a) What are the constraints with MOV instruction of 8086 microprocessor ? 4

   (b) Explain the construction of full adder using half adders. 6

(c) Write a 8086 assembly language program to interchange two bytes sized numbers stored at consecutive memory locations. 5

(d) List the differences between the following : 5

(i) LEA and MOV instructions in 8086

(ii) ROL and RCL instructions in 8086

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